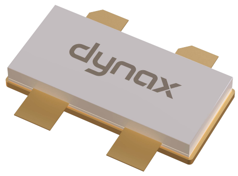
DXG2CH50A-200EF

RF Power GaN Transistor



1. Product profile

1.1 General description

DXG2CH50A-200EF is a 200 W RF GaN HEMT Transistor with second generation RF GaN technology from Dynax, which is ideal for cellular base station applications at frequencies from 4800 MHz to 5000 MHz.

Table 1. Typical performance [1]

Freq (MHz)	P_{sat} [2] (dBm)	P_{avg} [3] (dBm)	η_D [3] (%)	G_P [3] (dB)	ACPR [3] (dBc)
4800	53.3	44.5	44.2	14.0	-28.5/-47.5
4900	53.2	44.5	44.5	14.2	-28.5/-47.0
5000	53.1	44.5	44.6	14.2	-29.0/-45.5

[1] Typical Doherty performance in Dynax Demo with the device soldered onto the heatsink, test condition: V_{DS} = 48 V, I_{DQA} = 200 mA, V_{GSB} = - 4.8 V.

[2] Test condition: Input signal Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

[3] Test condition: Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF. ACPR measured in 3.84 MHz channel bandwidth @ ±5 MHz offset.

1.2 Features and benefits

- High efficiency, high gain
- Internally matched for broadband performance
- Designed for Digital Pre-Distortion error correction systems
- Optimized for Doherty applications

1.3 Applications

- RF power amplifier for base stations and multi carrier applications in the 4800 MHz to 5000 MHz frequency range

1.4 Lead-free and RoHS compliant

2. Pinning information

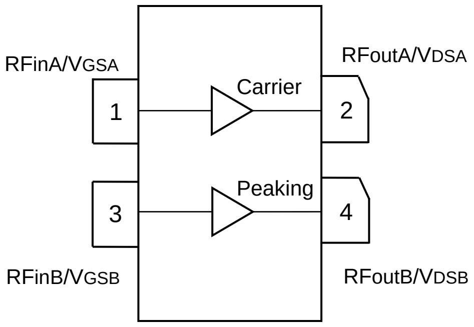


Fig 1. Pin configuration (Top view)

3. Ordering information

Table 2. Ordering information

Part number	Marking	Package type	Packaging information
DXG2CH50A-200EF	DXG2CH50A-200EF	780P2GB	Tray: Suffix = 20 units
			Tape and Reel: Suffix = 100 units; 44 mm Tape width; 13-inch Reel

4. Maximum ratings

Table 3. Maximum ratings

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DSS}	150	V
Gate-Source Voltage	V_{GS}	-10 ~ +2	V
Operating Voltage	V_{DS}	0 ~ +55	V
Maximum Forward Gate Current	I_{GMAX}	29.2	mA
Storage Temperature Range	T_{STG}	- 65 ~ +150	℃
Operating Junction Temperature	T_J	225	℃
Absolute Maximum Channel Temperature [1]	T_{MAX}	275	℃

[1] Functional operation above 225℃ has not been characterized and is not implied. Operation at T_{MAX} (275℃) reduces median time to failure by an order of magnitude; Operation beyond T_{MAX} could cause permanent damage.

5. Thermal characteristics

Table 4. Thermal characteristics

Parameter	Symbol	Value	Unit
Side A, Carrier			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 28.5 W	R_{thjc}(IR)	2.4	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 28.5 W	R_{thjc}(FEA)	3.3	℃/W
Side B, Peaking			
Thermal Resistance at Average Power by Infrared Measurement, Active Die Surface-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 7.1 W	R_{thjc}(IR)	0.2	℃/W
Thermal Resistance at Average Power by Finite Element Analysis, Junction-to-Case $T_{base\text{-}plate}$ = 85℃, P_D = 7.1 W	R_{thjc}(FEA)	0.3	℃/W

6. ESD protection characteristics

Table 5. ESD protection characteristics

Test Methodology	Class
Human Body Model (per JS-001-2012)	1A (≥ 250 V)
Charged Device Model (per JESD22-C101F)	C3 (≥ 1000 V)

7. Moisture sensitivity level

Table 6. Moisture sensitivity level

Test Methodology	Class
Moisture Sensitivity Level (per J-STD-020)	Level 1

8. Electrical characteristics (TA = 25℃ unless otherwise noted)

Table 7. DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Side A, Carrier					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	10.3	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 10.3 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 10.3 mA)	$V_{GS(th)}$	-4.0	-2.6	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 200 mA)	$V_{GS(Q)}$	-	-2.4	-	V
Side B, Peaking					
Drain-Source Leakage Current (V_{GS} = -10 V, V_{DS} = 150 V)	I_{DSS}	-	-	18.9	mA
Drain-Source Breakdown Voltage (V_{GS} = -10 V, I_D = 18.9 mA)	$V_{(BR)DSS}$	150	-	-	V
Gate Threshold Voltage (V_{DS} = 48 V, I_D = 18.9 mA)	$V_{GS(th)}$	-4.0	-2.6	-1.0	V
Gate Quiescent Voltage (V_{DS} = 48 V, I_D = 300 mA)	$V_{GS(Q)}$	-	-2.4	-	V

Table 8. RF characteristics (Typical Doherty performance – 5000 MHz) [1]

Parameter	Symbol	Min.	Typ.	Max.	Unit
Peak Output Power [2]	P_{sat}	51.7	52.7	-	dBm
Drain Efficiency [3]	η_D	34.9	41.9	-	%
Power Gain [3]	G_P	11.9	13.5	15.1	dB

[1] Typical Doherty performance in Dynax DXG2CH50A-200EF production test fixture, test condition: V_{DS} = 48 V, I_{DQA} = 200 mA, V_{GSB} = -3.0 V + V_{GSQ} @200 mA.

[2] Test condition: Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

[3] Test condition: P_{avg} = 44.5 dBm, Single-Carrier W-CDMA, IQ magnitude clipping, Input signal PAR = 7.5 dB @ 0.01 % probability on CCDF.

Table 9. Load mismatch

Parameter	Result
VSWR 10:1 at V_{DS} = 48 V, 200 W Pulsed CW output power, Pulse width = 100 μs, Duty cycle = 10%.	No device damage

9. Test information

9.1 Typical application circuit

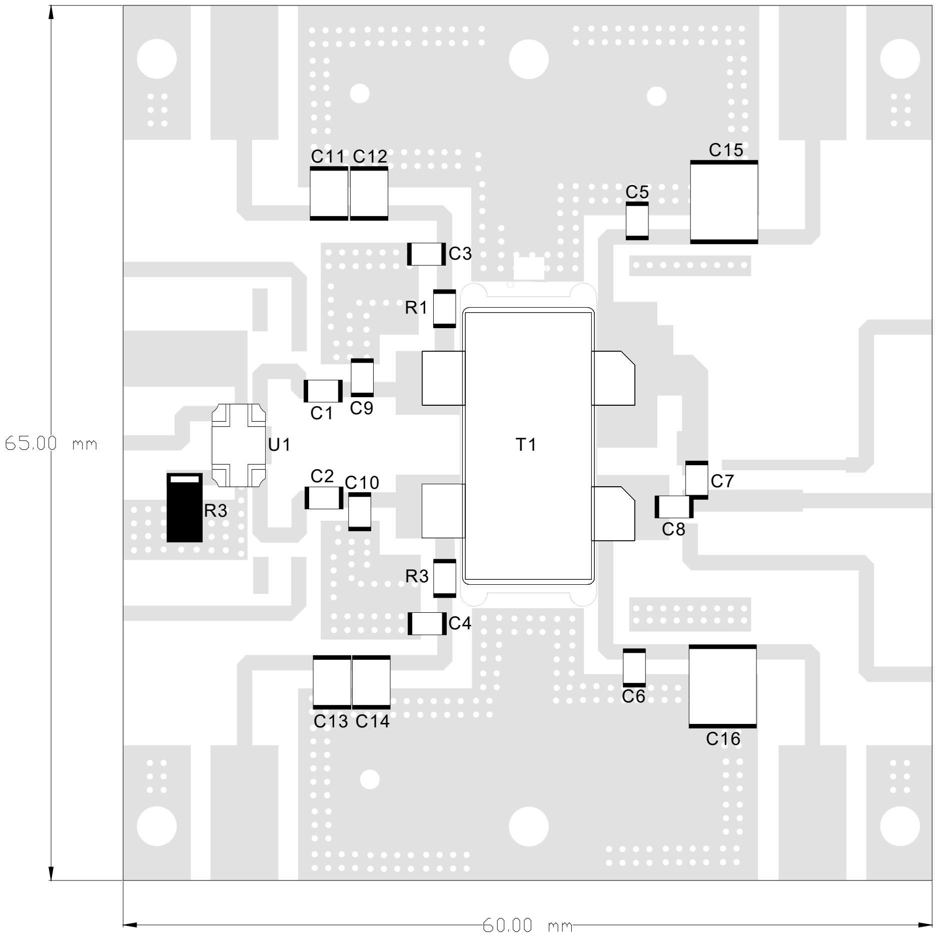


Fig 2. Component layout

Table 10. List of components

S/N	Type	Designator	Description	Value	Vendor
1	Cap	C1~C6	ATC600F3R9JT250XT	3.9 pF	ATC
2	Cap	C7~C8	ATC600F4R3JT250XT	4.3 pF	ATC
3	Cap	C9	ATC600F0R7JT250XT	0.7 pF	ATC
4	Cap	C10	ATC600F0R9JT250XT	0.9 pF	ATC
5	Cap	C11~C14	GRM32ER72A225KA35L	2.2 uF	Murata
6	Cap	C15~C16	C5750X7S2A106KT	10.0 uF	TDK
7	Res	R1,R2	RC1206FR_10R0	10 Ω	Yageo
8	Termination	R3	S1020A	50 Ω	RN2
9	HyBrid coupler	U1	CMX45E03	3 dB	RN2
10	Transistor	T1	DXG2CH50A-200EF	/	Dynax
11	PCB	/	Rogers 4350B	20 mil	Rogers

9.2 Graphic data

9.2.1 Pulsed CW

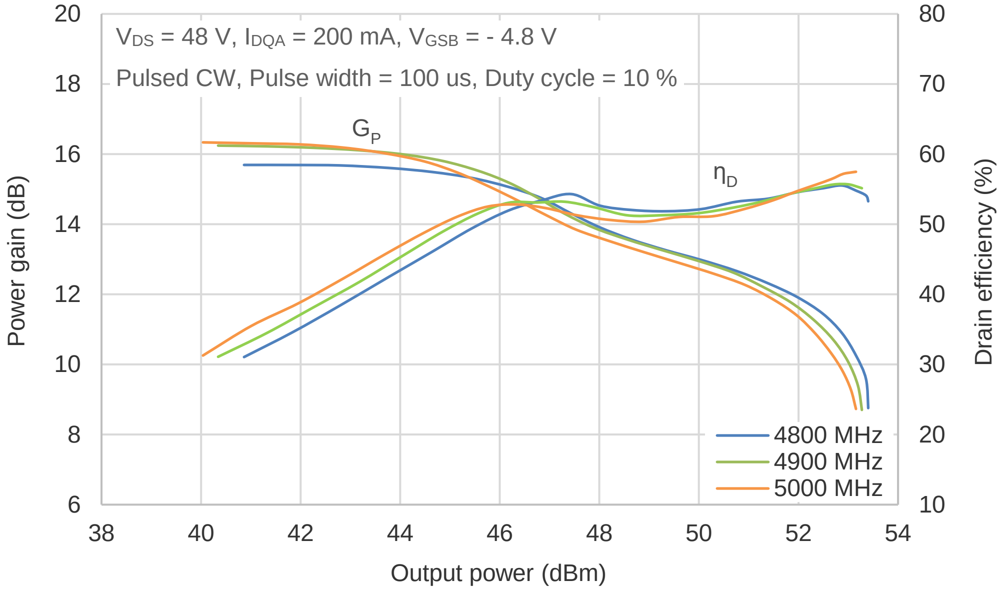


Fig 3. Power gain, Drain efficiency vs. Pulse output power

10. Impedance information

Table 11. Typical impedance of carrier [1]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
5000	24.4 - j1.8	6.0 - j12.5	16.8	50.3	107	63.1
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
5000	24.4 - j1.8	3.2 - 10.0	18.2	49.4	87	72.4

Table 12. Typical impedance of peaking [2]

Maximum Output Power						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
5000	15.8 + 3.8	5.2 - j13.9	16.5	51.6	145	61.8
Maximum Drain Efficiency						
Freq (MHz)	Z_S (Ω)	Z_L (Ω)	G_P (dB)	P_{sat} (dBm)	P_{sat} (W)	η_D (%)
5000	15.8 + 3.8	3.0 - j11.3	17.8	50.8	120	70.0

[1] V_{DS} = 48 V, I_{DQA} = 200 mA, Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

[2] V_{DS} = 48 V, I_{DQB} = 300 mA, Pulsed CW, Pulse width = 100 μs, Duty cycle = 10 %.

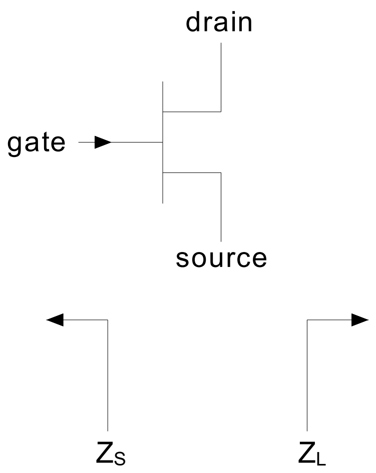


Fig 4. Definition of transistor impedance

11. Median lifetime

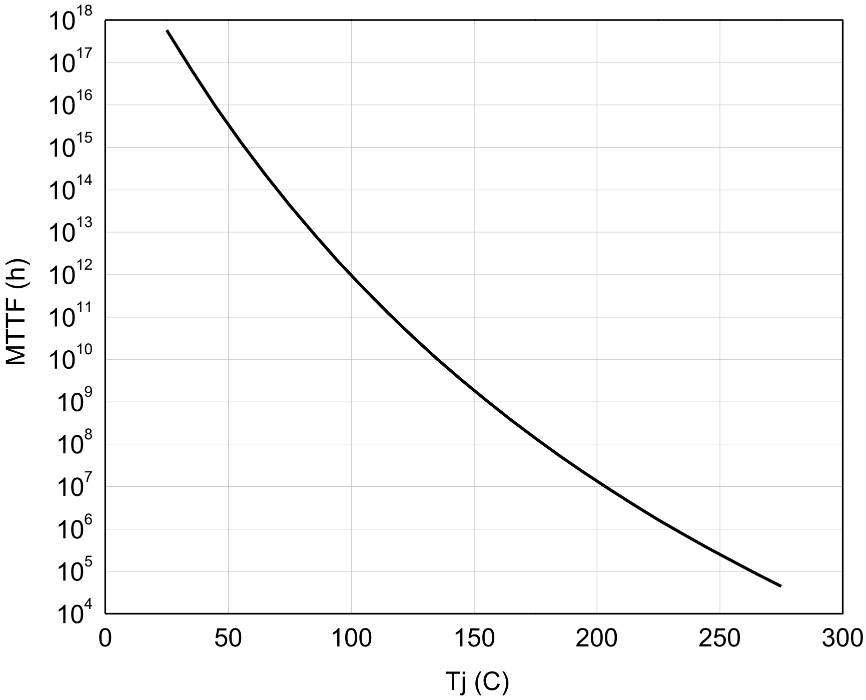


Fig 5. Median lifetime vs. channel temperature

12. Package outline

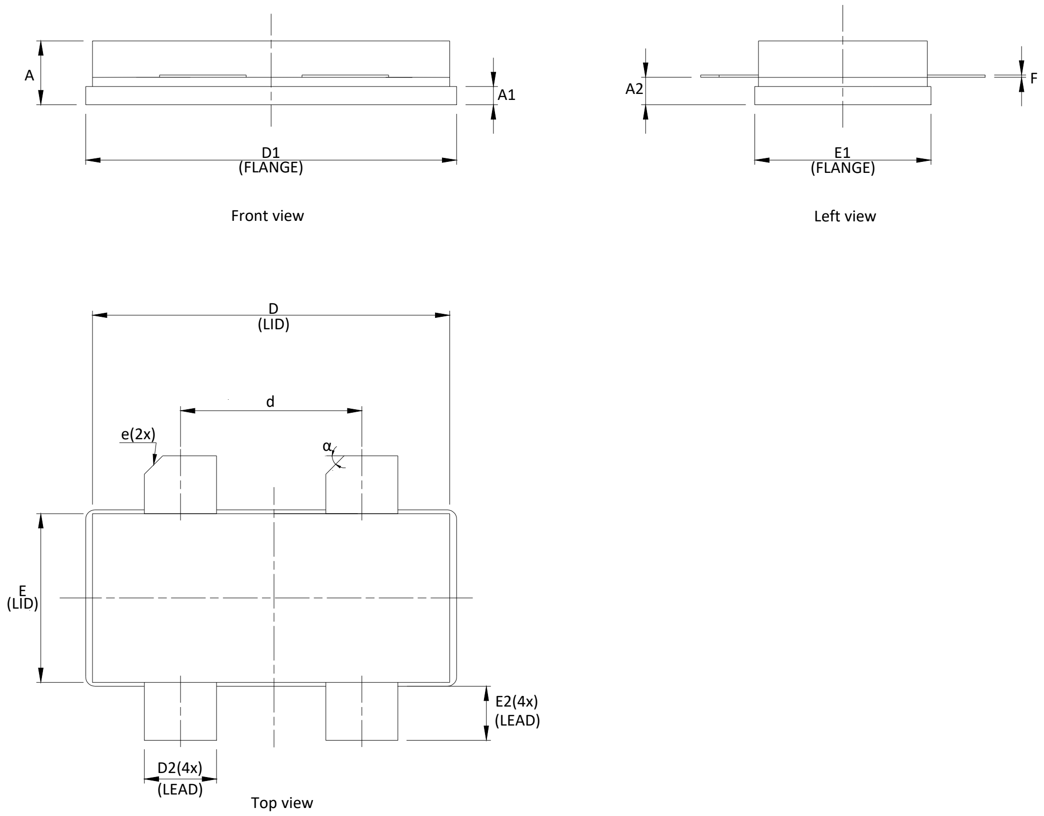


Fig 6. Package outline —— 780P2GB

Table 13. Package dimensions

DIM	INCH			MILLIMETER		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.134	0.144	0.154	3.40	3.65	3.90
A1	0.035	0.040	0.045	0.89	1.02	1.14
A2	0.057	0.062	0.067	1.45	1.58	1.70
D1	0.805	0.810	0.815	20.45	20.58	20.70
D2	0.153	0.158	0.162	3.87	4.00	4.13
d	0.385	0.390	0.395	9.77	9.90	10.03
D	0.772	0.780	0.788	19.61	19.82	20.02
E	0.365	0.370	0.375	9.27	9.40	9.53
E1	0.380	0.385	0.390	9.65	9.78	9.91
E2	0.098	0.118	0.138	2.50	3.00	3.50
F	0.003	0.005	0.006	0.08	0.12	0.15
e	TYP 0.04			TYP 1.02		
α	45° REF			45° REF		

13. Abbreviations

Table 14. Abbreviations

Acronym	Description
CW	Continuous Waveform
ESD	Electro-Static Discharge
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
MTTF	Median Time To Failure
VSWR	Voltage Standing Wave Ratio

14. Legal information

14.1 Datasheet status

Document status	Product status	Definition
Objective [short] datasheet	Engineering sample	This document contains data from the objective specification for product development.
Preliminary [short] datasheet	Engineering sample	This document contains data from the preliminary specification.
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